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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/075,113
Filing Date: February 13, 2002
Appellant(s): BEAUJOIN ET AL.

Paul J. Ditmyer
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 06/07/2006 appealing from the Office action mailed 03/07/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US-6108802	Kim et al.	08/22/2000
US-5751727	Martens	05/12/1998

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9, 11, 14-17, 20-23, 26-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US-6108802), hereinafter Kim, in view of Martens (US-5751727), hereinafter Martens.

<u>Claims 9, 11, 14, 20 and 26:</u>

Kim teaches a dual-port RAM-type FIFO memory device 100 (hereinafter referred to as the FIFO 100) comprised of a Random Access Memory (RAM) 102 that has n storage rows or words (shown in FIG. 3) where the input port 104 of the RAM 102

is connected to a Data Input Register (DIR) 108 and the output port 106 of the RAM 102 is connected to a Data Output Register (DOR) 110. Kim also teaches the FIFO 100 further includes a Write Address Register (WAR) 112 and a Read Address Register (RAR) 114 where each register 112 and 114 is M-bits wide, where M is an integer equal to the number of bits needed to address a RAM containing n words (a sequential access memory array storing p words each of n bits). (Col. 4, lines 34-50). Kim further teaches that BIST capability is provided by a BIST control 122 that controls a Test Pattern Generator (TPG) 118, which generates test patterns in the form of vectors for input to the RAM 102, and a Output Data Evaluator (ODE) 120. In addition, Kim teaches during testing intervals, multiplexer 121 passes test patterns from the TPG 118 to the DIR 108 for input to the RAM 102 (writing the memory array). Kim discloses that the ODE 120 is coupled to the output of the DOR 110 so as to receive the same data that is output to the Data Output (DO) line (extracting the p words from the data) and acts to compact or otherwise optimize the data output from the DO line during test intervals based on responses generated by the RAM 102 to the test patterns provided by the TPG 118 (comparing the test bits of the extracted test words with expected data bits). (Col. 6, lines 23-49). Kim does not explicitly teach the test words are "sequentially" extracted or compared. However, Kim does teach the Output Data Evaluator (ODE) 120 is coupled to the output of the Data Output Register (DOR) 110 so as to receive the same data that is output to the Data Output (DO) line (extracting the p words from the data). Martens teaches that it is necessary to have the capability to read data out of the array serially (sequentially extracting test words) in certain chip-testing conditions.

Martens teaches this capability, which is referred to as "scan testing" the array, requires that the array be able to hold its results in a group of memory elements where these memory elements are connected in series such that the output from the first memory element is fed to the scan input of the second element. Martens also teaches the output of the last memory element is fed to a test circuit outside the array (Kim's Output Data Evaluator (ODE) 120) for comparison to some expectation value. (Col. 5, lines 13-55, Fig. 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kim's Data Output Register (DOR) 110 with Martens' scan register configuration shown in Figure 4. The artisan would have been motivated to do so because it would enable Kim's Data Output Register (DOR) 110 to read data out of the array serially (sequentially extracting test words) and subsequently Kim's Output Data Evaluator (ODE) 120 will be able to compare the output test data sequentially before extracting the next test word. The artisan also would have been motivated to do so because Martens, in particular suggests it would be desirable to **improve the speed** of memory arrays utilized in high-speed ICs by utilizing the scannable dynamic latch circuit. However, in doing so the best overall combination of key criteria is realized: **minimum size**, **minimum delay**, and **proper testability** (i.e., scannability). (Col. 2, ll. 46-52, col. 8, ll. 47-52).

Claims 15, 21,and 27:

Martens teaches latch output of column n is depicted at line 128 and scan output n-1 is read to scan input n as depicted at line 132. (Col. 5, lines 51-53, Fig. 4). The first and second control means disclose in the claimed invention is a typical capture (first

control means) and shift (second control means) procedure which is commonly used in the art and would be obvious to one skilled in the art. The comparator means is taught by Kim in the Output Data Evaluator (ODE) 120. (Col. 6, lines 23-49).

<u>Claims 16, 22 and 28:</u>

This claim is rejected per claims 14, 20 and 26 above. Also, Martens teaches that the array scan latch organization of FIG. 4 includes multiple scannable latch circuits that are coupled to one another. (Col. 6, lines 23-49).

<u>Claims 17, 23 and 29:</u>

Kim teaches that the ODE 120 is coupled to the output of the DOR 110 so as to receive the same data that is output to the Data Output (DO) line (extracting the p words from the data) and acts to compact or otherwise optimize the data output from the DO line during test intervals based on responses generated by the RAM 102 to the test patterns provided by the TPG 118 (comparing the test bits of the extracted test words with expected data bits). (Col. 6, lines 23-49). Kim does not explicitly disclose that the ODE 120 includes XOR and XNOR gates. However, Kim does teach the ODE 120 compacts or optimizes the data that is compared. It is well known in the art that this procedure is accomplished through a XOR or XNOR logic and, therefore, is inherent in Kim's ODE 120.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US-6108802), hereinafter Kim, in view of Martens (US-5751727), hereinafter Martens, in further view of Zorian et al. (US-6330696), hereinafter Zorian.

Claim 12:

Kim does not explicitly teach the test words are written to obtain a checkerboard test pattern in the memory array. However, Kim does teach the RAM-type FIFO 100 may experience memory faults and functional faults associated with the RAM 102. (Col. 6, lines 66, 67, col. 7, line 1). Zorian teaches detection of junction leakage faults is accomplished by storing a pattern of alternating values in neighboring cells, such as storing a "checkerboard" pattern of"1"s and "0"s in the memory array. (Col. 4, lines 59-62, col. 6, lines 37-40, 46-51). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kim's fault detection algorithm to include Zorian's algorithm to detect junction leakage faults by writing a checkerboard pattern to the memory array. The artisan would have been motivated to do so because it would increase quality of the memory array test.

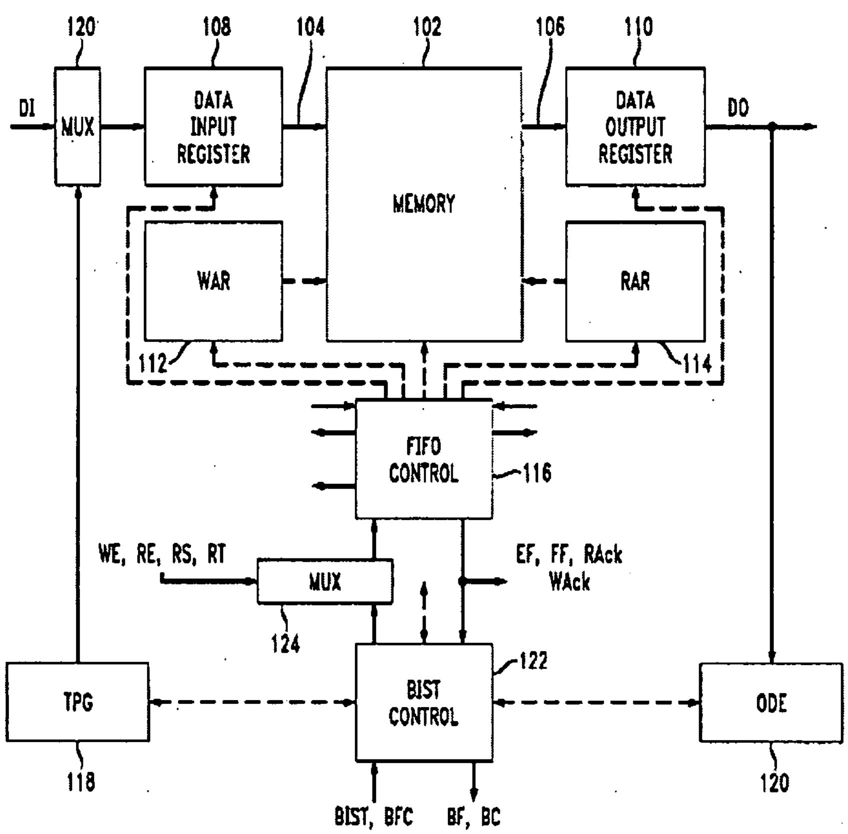
(10) Response to Argument

Whether or not independent claims 9, 11, 14, 20 and 26 are patentable over Kim et al. in view of Martens

The appellants argue on page 9 in referring to Kim et al. that, "there is no teaching of extracting the test words and comparing corresponding test bits with expected data bits as alleged by the Examiner. Indeed, Kim et al. specifically teaches that the output data compacted by the ODE 120 during test intervals takes the form of responses generated by the RAM 102 to the test patterns".

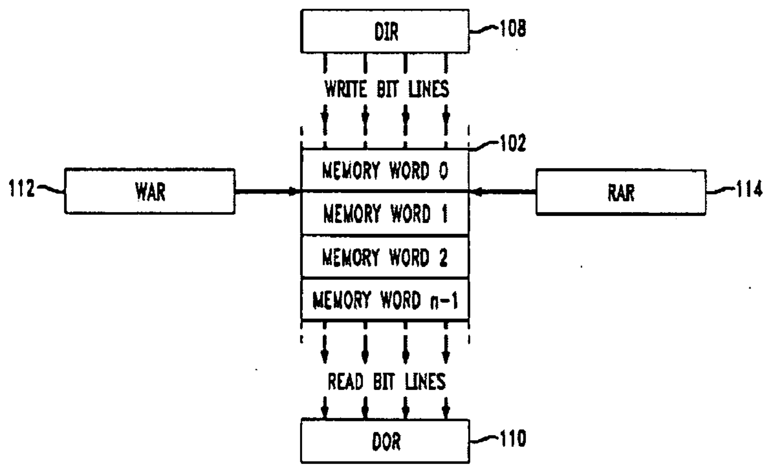
The Examiner disagrees and asserts that the appellants' mischaracterized this teaching of Kim et al. which states "*the Output Data Evaluator (ODE) 120 is coupled to the output of the Data Output Register (DOR) 110 so as to receive the same data that is output to the Data Output (DO) line (extracting the p words from the data) and acts to compact or otherwise optimize the data output from the DO line during test intervals* ***based on responses generated by the RAM 102 to the test patterns provided by the TPG 118***" (comparing the test bits of the extracted test words with expected data bits). (Col. 6, lines 23-49, Fig. 2).

FIG. 2



Kim et al. teaches ***extracting the test words*** when the outputs of the FIFO are loaded into the DOR 110 (see Fig. 3 below).

FIG. 3



Kim et al. teaches *comparing corresponding test bits with expected data bits* in that ODE 120 creates the BISTFlag (BF) (col. 6, ll. 57-61) by compacting or comparing the outputs of RAM 102 (**responses generated by the RAM 102**) with the expected values (**the test patterns provided by the TPG 118**).

The Examiner agrees, as presented in the Final Office Action of 03/07/2006, with appellants arguments on pages 9-10 that Kim et al. fail to teach *sequentially extracting* and *sequentially comparing* as claimed. This is what Martens teaches.

The appellants' argue on page 10, second paragraph, "nothing in Marten(s) et al. discloses testing a sequential access memory plane by sequentially extracting test words from the memory plane to sequentially compare with expected binary data bits, as claimed".

Firstly, the Examiner would like to show that serially scanning out data is the same as sequentially extracting test words. The "IEEE 100, The Authoritative Dictionary of IEEE Standard Terms, 7th Edition" defines the following terms on pages 1004, 1028 and 1029:

Scan (1) (general) To examine sequentially part by part.

(4) (data management) To examine a set of items sequentially.

(7) To examine stored information sequentially, part by part.

Serial (1) (A) Pertaining to the time sequencing of two or more processes.

(3) One bit following another over a single pathway.

Sequential (3) Pertaining to a circuit whose output values, at a given instant, depend upon its input values and internal state at that instant, and whose internal state depends on the immediately preceding input values and the preceding state.

The Examiner disagrees and asserts that it is the combination of Kim et al. (hereinafter Kim) and Martens that teach the features of the appellants' invention recited above. Martens teaches that "*it is necessary to have the capability to read data out of the array serially* (sequentially extracting test words) *in certain chip-testing conditions*". Martens teaches "*this capability, which is referred to as "scan testing" the array, requires that the array be able to hold its results in a group of memory elements where these memory elements are connected in series such that the output from the first memory element is fed to the scan input of the second element*".

The Examiner contends that it is well known in the art that serial scan chains, as disclosed in Martens, serially or sequentially shift the contents of the registers (memory elements) out of the last register through a single Scan Out (SO) signal so the sequentially extracted data can be evaluated (Martens, Fig. 4, Scan Out_n fed to Test Circuit Input). Martens Fig. 4 is shown below.

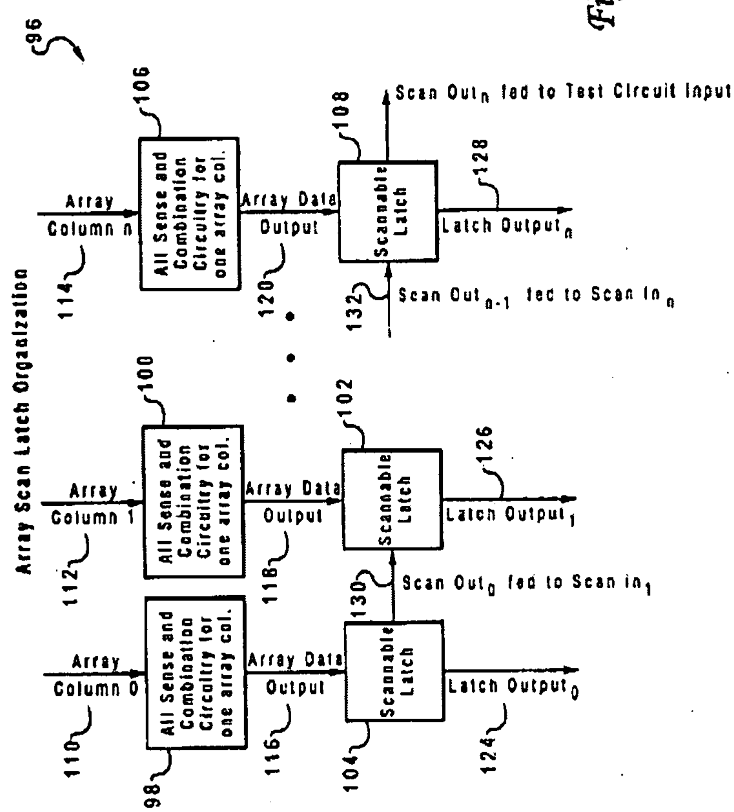


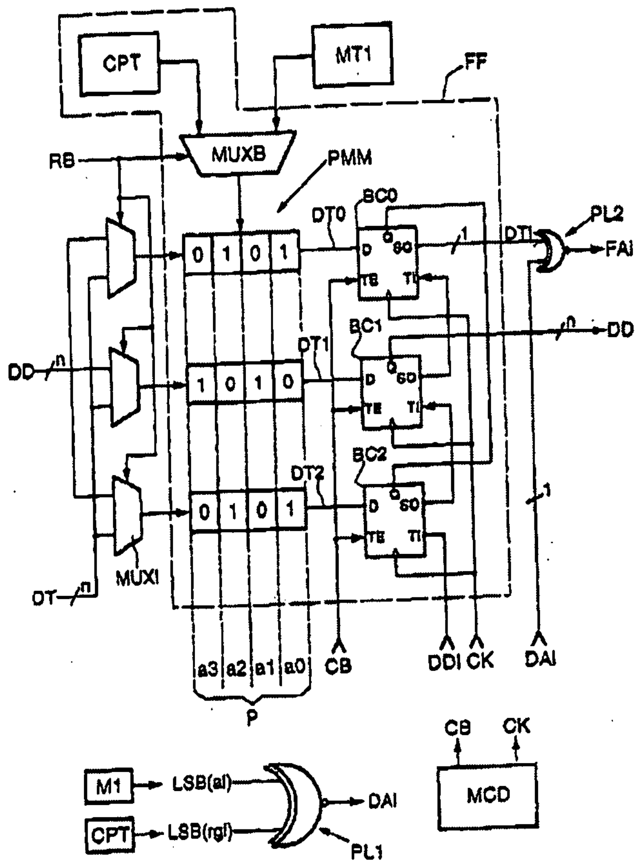
Fig. 4

This is performed in response to a SCAN/ sequentially clocking the registers (sequentially extracting test words from the memory plane). (see col. 8. ll. 24-39). Martens also teaches *sequentially comparing with expected binary data bits* in that "*the*

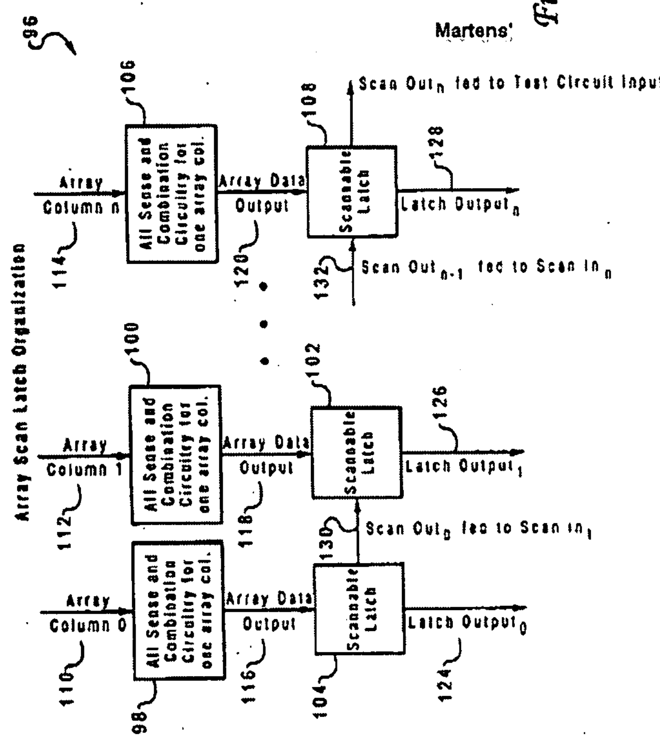
output of the last memory element is fed to a test circuit outside the array for comparison to some expectation value".

The Examiner asserts that the comparison must be sequential, even though not explicitly stated, because the data being sequentially shifted out of SO output can only be compared serially/sequentially. The Examiner asserts that the combination of Martens' method of "scan testing" (sequentially extracting and comparing) a memory array with Kim's extracting of test words and comparing them to expected values yields a memory array which is sequentially read and those outputs, being fed into the Kim's Output Data Evaluator (ODE) 120, are sequentially compared with expected values and would have been perfectly obvious to one of ordinary skill in the art at the time the invention was made. Further, the Examiner would also like to point out the similarities between Appellants' Fig. 1 and Martens' Fig. 4, shown below, where elements 104, 102 and 103 of Martens' Fig. 4 correlates to BC0, BC1 and BC2 of Appellants' Fig. 1 for sequentially extracting the test words from the memory array.

Appellants' FIG.1



Martens' Fig. 4



Appellants state on page 11, paragraph 2, "*the Examiner is impermissibly using the teachings of Appellants' own patent application as a roadmap to modify the prior art*".

In response to Appellants' argument that the Examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the Appellants' disclosure, such a

reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Further, the Examiner contends that scannable memories are well known in the art for the purpose of testing the memory and examining the contents. Martens, in particular suggests it would be desirable to **improve the speed** of memory arrays utilized in high-speed ICs by utilizing the scannable dynamic latch circuit. However, in doing so the best overall combination of key criteria is realized: **minimum size**, **minimum delay**, and **proper testability** (i.e., scannability). (Col. 2, ll. 46-52, col. 8, ll. 47-52). The motivation to modify Kim's memory is clearly stated in Martens and, as such, satisfies the "motivation to combine" Appellants' arguments presented on pages 11-12.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

John J. Tabone Jr. 4/26/07

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Conferees:

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